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*Sub E*  
C<sup>1</sup>

1. (Amended) A transistor comprising:  
a channel region;  
a first gate on top of said channel region;  
a second gate below said channel region; and  
an isolation layer below said second gate,  
wherein said first gate and said second gate are self-aligned and electrically separated  
from each other.

C<sup>2</sup>

11. (Amended) A semiconductor chip having at least one transistor, said transistor  
comprising:  
a channel region;  
a first gate on top of said channel region;  
a second gate below said channel region; and  
an isolation layer below said second gate,  
wherein said first gate is self-aligned with and comprises a different material than said  
second gate.

Please cancel claims 21-43.

*Sub E*  
C<sup>3</sup> Please add the following new claims:

44. A transistor comprising:  
a channel region;  
a first gate on top of said channel region;  
a second gate below said channel region;  
an isolation layer below said second gate; and  
source and drain regions laterally adjacent said channel region,

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7 wherein said source and drain regions are self-aligned with said first gate and said second  
8 gate, such that said source and drain regions do not horizontally overlap said first gate or said  
9 second gate, and

10 wherein said first gate and said second gate are electrically separated from each other.

1 45. A transistor comprising:

2 a channel region;

3 a first gate on top of said channel region;

4 a second gate below said channel region;

5 an isolation layer below said second gate; and

6 source and drain regions laterally adjacent said channel region, said first gate, and said  
7 second gate,

8 wherein said first gate and said second gate are electrically separated from each other.

1 46. The transistor in claim 1, wherein said self-aligned nature of said first gate and said  
2 second gate positions said first gate above and aligned with said second gate.

1 47. The transistor in claim 4, further comprising:

2 source and drain regions laterally adjacent said channel region, said first gate, and said  
3 second gate; and

4 source and drain dielectrics between said source and drain regions and said first gate and  
5 said second gate,

6 wherein a thickness and material selection of said first gate dielectric and said second  
7 gate dielectric is independent of said source and drain dielectrics.

1 48. The semiconductor chip in claim 11, further comprising source and drain regions laterally  
2 adjacent said channel region, wherein said source and drain regions are self-aligned with said

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3 first gate and said second gate, such that said source and drain regions do not horizontally  
4 overlap said first gate or said second gate.

1 49. The semiconductor chip in claim 11, wherein said self-aligned nature of said first gate  
2 and said second gate positions said first gate above and aligned with said second gate.

1 50. The semiconductor chip in claim 11, further comprising source and drain regions laterally  
2 adjacent said channel region, said first gate, and said second gate.

1 51. The semiconductor chip in claim 14, further comprising:  
2 source and drain regions laterally adjacent said channel region, said first gate, and said  
3 second gate; and  
4 source and drain dielectrics between said source and drain regions and said first gate and  
5 said second gate,  
6 wherein a thickness and material selection of said first gate dielectric and said second  
7 gate dielectric is independent of said source and drain dielectrics.

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